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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,680	07/28/2004	Brent A. Anderson	BUR920040049US1	4309

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,680	ANDERSON ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *15-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0704*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 07/28/2004 through 01/06/2006.

Claims 1-28 are active in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

a. Information Disclosure Statement (IDS) filed on 07/28/2004. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

b. Applicant made a provisional election without traverse to prosecute the invention of Group II, claims 1-14, drawn to semiconductor device(s) in the Response to Restriction Requirement filed 01/06/2006.

Claims 15-28 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected group there being no allowable generic or linking claim.

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

Specification

3. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim(s) 1, 5, 6, 8, 12, and 13 is/are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent Application Publication No. 2005/0242391 by She et al.

Regarding claim 1, She discloses a multiple-gate transistor, as shown in figs. 10-11, comprising:

a channel region (between source and drain regions);

a logic gate (Gate 1) adjacent a first side (lower side) of said channel region;

a floating gate (trapping layer, where Bit 1 and Bit 2 are trapped) adjacent a second side (upper side) of said channel region, wherein said first side is opposite said second side; and

a programming gate (gate 2 with dark region) adjacent said floating gate, wherein said floating gate is between said programming gate and said channel region.

Regarding claim 8, Hsu discloses a multiple-gate transistor, as shown in figs. 10-11, comprising:

a channel region; source and drain regions at ends of said channel region;

a gate oxide (tunnel oxide) on a first side (lower side) of said channel region;

a logic gate (gate 1) adjacent said first gate oxide, wherein said gate oxide is between said logic gate and said channel region;

a first insulator (between channel region and the region where Bit 1 and Bit 2 being trapped) on a second side (upper side) of said channel region, wherein said second side of said channel region is opposite said first side;

a floating gate (trapping layer, where Bit 1 and Bit 2 are trapped) adjacent said first insulator wherein said first insulator is between said floating gate and said channel region;

a second insulator (between the trapping layer and gate 2 with dark region) adjacent said floating gate; and

a programming gate (gate 2 with dark region) adjacent said second insulator wherein said second insulator is between said programming gate and said floating gate.

Regarding claims 5, and 12, She discloses the transistor wherein said transistor comprises a fin-type field effect transistor (FinFET). See figs. 8-11.

Regarding claims 6, and 13, She discloses the transistor further comprising source and drain regions at ends of said channel region, wherein said channel region comprises the middle portion of a fin structure and said source and drain regions comprise end portions of said fin structure. See figs. 8-11.

6. Claim(s) 1, 3, 4, 7, 8, 10, 11, and 14 is/are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,107,141 to Hsu et al.

Regarding claim 1, Hsu discloses a multiple-gate transistor, as shown in figs. 1, 2, and 9, comprising:

a channel region (between source 20 and drain 20;

a logic gate 120 adjacent a first side (left side) of said channel region;

a floating gate 130 adjacent a second side (right side) of said channel region, wherein said first side is opposite said second side; and

a programming gate 140 adjacent said floating gate 130, wherein said floating gate 130 is between said programming gate 140 and said channel region.

Regarding claim 8, Hsu discloses a multiple-gate transistor, as shown in figs. 1, comprising:

a channel region; source and drain regions 30/20 at ends of said channel region;

a gate oxide 232 on a first side (left side) of said channel region;

a logic gate 120 adjacent said first gate oxide 232, wherein said gate oxide 232 is between said logic gate 120 and said channel region;

a first insulator 235 on a second side (right side) of said channel region, wherein said second side of said channel region is opposite said first side;

a floating gate 130 adjacent said first insulator 235, wherein said first insulator 235 is between said floating gate 130 and said channel region;

a second insulator 237 adjacent said floating gate 130; and

a programming gate 140 adjacent said second insulator 237, wherein said second insulator 237 is between said programming gate 140 and said floating gate 130.

Regarding claims 3 and 10, Hsu discloses the transistor wherein voltage in said logic gate 120 causes said transistor to switch on and off. Col. 1 line 66 to col. 2, line 1 state(s) that logic or select gate 120 serves the standard electrical function of permitting access to the cell. Thus, controlling the voltage applied to the logic gate 120 would control the access to the cell, or would turn the cell on and off.

Regarding claims 4 and 11, Hsu discloses the transistor wherein charge in said floating gate 130 adjusts the threshold voltage of said transistor. This is inherent since a charge in the floating gate 130 would create an electric field in the insulator 235; therefore, such charge would effect the threshold voltage of the transistor.

Regarding claims 7 and 14, Hsu discloses the transistor wherein said floating gate 130 is electrically insulated from other structures. See fig. 1.

Claim Rejections - 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim(s) 2 and 9 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. U.S. Patent No. 6,107,141 to Hsu et al.

Regarding claims 2 and 9, Hsu discloses the transistor comprising all claimed limitations, including a gate oxide 232 between said channel region and said logic gate 120 and a first insulator 235 between said channel region and said floating gate 130, except for expressly teaching that the first insulator 235 is thicker than the gate oxide 232.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the thicknesses of the gate oxide layer 232 and the first insulating layer 235 are significantly depending on (the dielectric constant of) the materials being used to form each of them; and selecting a known material on the basis

of its suitability for the intended use is just within the general skill of a worker in the art. In re Leshin, 125 USPQ. Furthermore, a modification to have a thickness of one layer to be thicker or thinner than that of the other layer would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Conclusion

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

Dao H. Nguyen
Art Unit 2818
February 28, 2006

David Nelms
Supervisory Patent Examiner
Technology Center 2800